What is claimed is:

1. A method of performing a dot product operation with rounding and shifting in a microprocessor in response to a single rounding dot product instruction, the method comprising the steps of:

fetching a first pair of elements and a second pair of elements;

forming a first product of the first pair of elements and a second product of the second pair of elements;

combining the first product with the second product to form a combined product;

rounding the combined product to form an intermediate result; and

shifting the intermediate result a selected amount to form a final result.

2. The method of Claim 1, wherein the step of shifting truncates a selected number of least significant bits of the intermediate result.

3. The method of Claim 2, wherein the step of rounding adds a rounding value to the combined product to form the intermediate result, and wherein the step of shifting shifts the intermediate result right by a selected shift amount.

4. The method of Claim 3, wherein the rounding value is 2**n and the selected shift amount is n+1.

5. The method of Claim 4, wherein n has a fixed value of fifteen.

6. The method of Claim 1, wherein the step of rounding treats the intermediate result as a signed integer, such that when an overflow occurs,

the intermediate result will wrap from a largest positive value to a smallest negative value.

7. The method of Claim 6, wherein an overflow is not reported.

8. The method of Claim 1, wherein the step of fetching comprises the steps of:

fetching a first operand;

fetching a second operand;

extracting one of the first pair of elements and one of the second pair of elements from the first operand; and

extracting another one of the first pair of elements and another one of the second pair of elements from the second operand.

9. The method of Claim 1, wherein the step of forming treats a one of the first pair of elements as a signed number value and treats another one of the first pair of elements as an unsigned number value.

10. The method of Claim 1, wherein the step of combining comprises subtracting the product of second pair of elements from the product of first pair of elements.

11. The method of Claim 1, wherein the step of combining comprises adding the product of second pair of elements to the product of first pair of elements.

12. The method of Claim 1, wherein the steps of forming and combining operate on a plurality of pairs of elements.

13. A digital system having a microprocessor operable to execute a rounding dot product instruction, wherein the microprocessor comprises:

storage circuitry for holding pairs of elements;

a multiply circuit connected to receive a first number of pairs of elements from the storage circuitry in a first execution phase of the microprocessor responsive to the dot product instruction, the multiply circuit comprising a plurality of multipliers equal to the first number of pairs of elements;

an arithmetic circuit connected to receive a plurality of products from the plurality of multipliers, the arithmetic circuit having a provision for mid-position rounding responsive to the rounding dot product instruction; and

a shifter connected to receive an output of the arithmetic circuit, the shifter operable to shift a selected amount in response to the rounding dot product instructions.

14. The digital system of Claim 13, wherein the arithmetic circuit has a carry input connected to a mid-position, wherein the carry input is asserted in response to the rounding dot product instruction.

15. The digital system according to Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the processor via a keyboard adapter;

a display, connected to the processor via a display adapter;

radio frequency (RF) circuitry connected to the processor; and

an aerial connected to the RF circuitry.